

1 CLAIMS:

2 1. A method of forming a capacitor comprising the following
3 steps:

4 providing a node to which electrical connection to a first capacitor
5 plate is to be made;

6 providing a first layer of material over the node, the first layer
7 of material being selectively etchable relative to the node;

8 providing a second layer of material over the first layer, the
9 second layer of material being selectively etchable relative to the first
10 layer of material and being electrically conductive;

11 providing a first masking layer over the second layer of material;

12 etching a first opening into the first masking layer over the node;

13 providing a second masking layer over the first masking layer to
14 a thickness which less than completely fills the first opening;

15 anisotropically etching the second masking layer to define a spacer
16 received laterally within the first opening and thereby defining a second
17 opening relative to the first masking layer which is smaller than the
18 first opening;

19 after anisotropically etching the second masking layer, etching
20 unmasked first masking layer material away;

21 after anisotropically etching the second masking layer, selectively
22 anisotropically etching the second layer of material relative to the first
23 layer of material;
24

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1 after etching the second layer material, selectively etching the first
2 layer of material relative to the node to effectively extend the second
3 opening to the node and define an outline of the first capacitor plate
4 using the spacer as an etching mask;

5 plugging the extended second opening with an electrically
6 conductive plugging material, the plugging material electrically
7 interconnecting the node and second layer;

8 after extending the second opening to the node, selectively
9 isotropically etching the first layer material relative to the second layer
10 material; and

11 providing a capacitor dielectric layer and a conductive second
12 capacitor plate layer over the conductive second layer.

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14 2. The method of forming a capacitor of claim 1 wherein the
15 first opening is provided to have a minimum opening width equal to
16 the minimum capable photolithographic feature dimension at the time
17 of fabrication, the second opening thereby having a minimum opening
18 width which is less than the minimum capable photolithographic feature
19 dimension at the time of fabrication, the resultant plugging material
20 plugging the second opening thereby having a minimum width which is
21 less than the minimum capable photolithographic feature dimension at
22 the time of fabrication.
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1 3. The method of forming a capacitor of claim 1 wherein the
2 unmasked first masking layer is etched before extending the second
3 opening to the node.

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5 4. The method of forming a capacitor of claim 1 wherein the
6 unmasked first masking layer is etched after extending the second
7 opening to the node.

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9 5. The method of forming a capacitor of claim 1 wherein only
10 one photomasking step is utilized to define the first capacitor plate
11 between the step of providing the node and the step of providing the
12 capacitor dielectric layer.

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14 6. The method of forming a capacitor of claim 1 wherein the
15 node comprises an outer surface of a pillar which projects from a
16 diffusion region provided in a bulk semiconductive substrate.

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18 7. The method of forming a capacitor of claim 1 wherein the
19 first layer is electrically insulative.

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21 8. The method of forming a capacitor of claim 1 wherein the
22 first layer predominately comprises SiO_2 .

1 9. The method of forming a capacitor of claim 1 wherein the
2 second layer material constitutes the same material as that of the node.

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4 10. The method of forming a capacitor of claim 1 wherein the
5 plugging material, the node and the second layer of material all
6 constitute the same material.

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8 11. The method of forming a capacitor of claim 1 wherein the
9 second masking material comprises Si_3N_4 .

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11 12. The method of forming a capacitor of claim 1 further
12 comprising after selectively etching the first layer, etching the spacer
13 away.

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15 13. The method of forming a capacitor of claim 1 wherein the
16 step of selectively etching the first layer comprises anisotropically etching
17 the first layer.

18
19 14. The method of forming a capacitor of claim 1 wherein,
20 the node comprises an outer surface of a pillar which projects
21 from a diffusion region provided in a bulk semiconductive substrate; and
22 the first layer is electrically insulative.
23
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15. The method of forming a capacitor of claim 1 wherein,
the node comprises an outer surface of a pillar which projects
from a diffusion region provided in a bulk semiconductive substrate;
the first layer is electrically insulative; and
further comprising after selectively etching the first layer, etching
the spacer away.

16. The method of forming a capacitor of claim 1 wherein,
the node comprises an outer surface of a pillar which projects
from a diffusion region provided in a bulk semiconductive substrate;
the first layer is electrically insulative;
further comprising after selectively etching the first layer, etching
the spacer away; and

wherein the plugging material, the node and the second layer of
material all constitute the same material.

17. The method of forming a capacitor of claim 1 comprising etching the first masking layer away before anisotropically etching the second layer material, and then further comprising:

providing a third masking layer over the spacer;

anisotropically etching the third masking layer to form a secondary spacer laterally outward of the first stated spacer; and

using said spacers collectively as an etching mask during the second and first layer etchings.

18. The method of forming a capacitor of claim 17 further comprising forming at least two of said capacitors, the two capacitors being adjacent one another and having a minimum spacing from one another which is less than the minimum capable photolithographic feature dimension at the time of fabrication.

19. The method of forming a capacitor of claim 1 further comprising providing a plurality of alternating of the first and second layers outwardly relative to the node, and providing the first and second masking layers and first and second openings outwardly thereof;

the method further comprising alternately anisotropically etching the respective second and first layers to extend the second opening therethrough to the node; and

the step of isotropically etching the first layer material relative to the second layer material defining a plurality of laterally projecting electrically conductive second layer fins.

20. The method of forming a capacitor of claim 19 wherein only one photomasking step is utilized to define the first capacitor plate between the step of providing the node and the step of providing the capacitor dielectric layer.

21. The method of forming a capacitor of claim 19 wherein the node comprises an outer surface of a pillar which projects from a diffusion region provided in a bulk semiconductive substrate.

22. The method of forming a capacitor of claim 19 wherein the first layer is electrically insulative.

1 23. The method of forming a capacitor of claim 19 wherein the
2 plugging material, the node and the second layer material all constitute
3 the same material.

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5 24. The method of forming a capacitor of claim 19 further
6 comprising after selectively etching the first layer, etching the spacer
7 away.

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9 25. The method of forming a capacitor of claim 19 comprising
10 etching the first masking layer away before anisotropically etching the
11 second layer material, and then further comprising:

12 providing a third masking layer over the spacer;

13 anisotropically etching the third masking layer to form a secondary
14 spacer laterally outward of the first stated spacer; and

15 using said spacers collectively as an etching mask during the
16 second and first layer etchings.

17
18 26. The method of forming a capacitor of claim 19 wherein,
19 the node comprises an outer surface of a pillar which projects
20 from a diffusion region provided in a bulk semiconductive substrate; and
21 the first layer is electrically insulative.
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1 27. The method of forming a capacitor of claim 19 wherein,
2 the node comprises an outer surface of a pillar which projects
3 from a diffusion region provided in a bulk semiconductive substrate;
4 the first layer is electrically insulative; and
5 further comprising after selectively etching the first layer, etching
6 the spacer away.

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8 28. The method of forming a capacitor of claim 19 wherein,
9 the node comprises an outer surface of a pillar which projects
10 from a diffusion region provided in a bulk semiconductive substrate;
11 the first layer is electrically insulative;
12 further comprising after selectively etching the first layer, etching
13 the spacer away; and
14 wherein the plugging material, the node and the second layer of
15 material all constitute the same material.

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17 29. A capacitor produced according to the method of claim 1.
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1 30. A method of forming a capacitor comprising the following
2 steps:

3 providing a node to which electrical connection to a first capacitor
4 plate is to be made;

5 providing a layer of conductive material outwardly of the node;

6 providing a first masking layer over the conductive material layer;

7 etching a first opening into the first masking layer over the node;

8 providing a second masking layer over the first masking layer to
9 a thickness which less than completely fills the first opening;

10 anisotropically etching the second masking layer to define a spacer
11 received laterally within the first opening and thereby defining a second
12 opening relative to the first masking layer which is smaller than the
13 first opening;

14 after anisotropically etching the second masking layer, etching
15 unmasked first masking layer material away;

16 after anisotropically etching the second masking layer, etching
17 through the conductive material layer to extend the second opening to
18 the node, the node and conductive layer being electrically isolated from
19 one another after the conductive material layer etching;

20 plugging the extended second opening with an electrically
21 conductive plugging material, the plugging material electrically
22 interconnecting the node and conductive layer; and

23 providing a capacitor dielectric layer and a conductive second
24 capacitor plate layer over the conductive layer.

1 31. The method of forming a capacitor of claim 30 wherein the
2 first opening is provided to have a minimum opening width equal to
3 the minimum capable photolithographic feature dimension at the time
4 of fabrication, the second opening thereby having a minimum opening
5 width which is less than the minimum capable photolithographic feature
6 dimension at the time of fabrication, the resultant plugging material
7 plugging the second opening thereby having a minimum width which is
8 less than the minimum capable photolithographic feature dimension at
9 the time of fabrication.

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11 32. The method of forming a capacitor of claim 30 wherein only
12 one photomasking step is utilized to define the first capacitor plate
13 between the step of providing the node and the step of providing the
14 capacitor dielectric layer.

15
16 33. The method of forming a capacitor of claim 30 wherein the
17 node comprises an outer surface of a pillar which projects from a
18 diffusion region provided in a bulk semiconductive substrate.

19
20 34. The method of forming a capacitor of claim 30 wherein the
21 conductive material layer constitutes the same material as that of the
22 node.

1 35. The method of forming a capacitor of claim 30 wherein the
2 plugging material, the node and the conductive material layer all
3 constitute the same material.

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5 36. The method of forming a capacitor of claim 30 wherein the
6 second masking material comprises Si_3N_4 .

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8 37. The method of forming a capacitor of claim 30 further
9 comprising after etching through the conductive material layer, etching
10 the spacer away.

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12 38. The method of forming a capacitor of claim 30 comprising
13 etching the first masking layer away before etching through the
14 conductive layer material, and then further comprising:

15 providing a third masking layer over the spacer;

16 anisotropically etching the third masking layer to form a secondary
17 spacer laterally outward of the first stated spacer; and

18 using said spacers collectively as an etching mask during the
19 second and first layer etchings.

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21 39. A capacitor produced according to the method of claim 30.
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1 40. A method of forming a capacitor comprising the following
2 steps:

3 providing a node to which electrical connection to a first capacitor
4 plate is to be made;

5 after providing the node, providing a finned lower capacitor plate
6 in ohmic electrical connection with the node using no more than one
7 photomasking step; and

8 providing a capacitor dielectric layer and a conductive second
9 capacitor plate layer over the conductive layer.

10
11 41. The method of forming a capacitor of claim 40 wherein the
12 node comprises an outer surface of a pillar which projects from a
13 diffusion region provided in a bulk semiconductive substrate.

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15 42. The method of forming a capacitor of claim 40 wherein the
16 finned lower capacitor plate constitutes the same material as that of the
17 node.

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1 43. A capacitor construction comprising:

2 a stem; and

3 at least two laterally opposed fins interconnected with and
4 projecting laterally from the stem, the stem having a minimum width
5 which is less than the minimum capable photolithographic feature
6 dimension at the time of fabrication.

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8 44. A pair of adjacent capacitors fabricated relative to a
9 semiconductor substrate, the adjacent capacitors having a minimum
10 lateral spacing from one another which is less than the minimum
11 capable photolithographic feature dimension at the time of fabrication.

12
13 45. The capacitors of claim 44 wherein each comprises:

14 a stem; and

15 at least two laterally opposed fins interconnected with and
16 projecting laterally from the stem, the stem having a minimum width
17 which is less than the minimum capable photolithographic feature
18 dimension at the time of fabrication.